1. Perform the following multiplications using the 4-bit 2’s complement floating-point format. Normalize the result and verify your answer in Base 10.

   a) \((3/8 \times 2^3) \times (-1/2 \times 2^{-1}) = ?\)
   
   b) \(F_1 = 1.011, E_1 = 0101\)
   \(F_2 = 1.010, E_2 = 0011\)
   \(N_1 \times N_2 = ?\)

2. Represent the following decimal numbers in the IEEE single precision floating-point format:

   a) \(25.25_{10}\)
   b) \(-7.5_{10}\)
   c) \(-63.125_{10}\)

3. Write a structural VHDL model for an \(N\)-bit serial-in, serial-out shift register with inputs SI (serial input), EN (enable), and CK (clock), and a serial output (SO). Your model should include a generic in the entity declaration and a generate statement in the architecture. Assume that the following component for a D flip-flop with enable is available.

   ```vhdl
   component DFF
       port(D, EN, CK: in std_logic;
           Q: out std_logic);
   end component;
   ```

   a. Draw a block diagram and label all signals (internal and external).
   b. Write the VHDL model.