1. Design a 4-bit linear feedback shift register (LFSR) where \( Q^+ = (Q_1 \oplus Q_0) \& Q_{3:1} \). The circuit can perform basic encryption of a data byte \( D \) by shifting it \( N \) times. When \( St = 1 \), \( D \) is loaded into the 4-bit register and \( N \) is loaded into a 4-bit down counter. The register then shifts until the counter reaches 0, when \( Done \) is signaled.

   a) Illustrate the encryption of the following sample data:
      - \( D = 0011 \), \( N = 5 \)
   b) Draw a block diagram of the LFSR circuit and define any necessary control signals.
   c) Draw the state graph for the control circuit.
   d) Write a complete VHDL model (entity and behavioral architecture) for the LFSR. Use two processes: one to generate the control signals and one to update the registers based on those signals.

2. Given the block diagram for the signed 2’s complement multiplier below, show the contents of registers \( A \) and \( B \) for each clock cycle when the multiplicand = \(-3/8\) and the multiplier = \(-3/4\). Verify your answer.