1. Given the following logic circuit:

![Logic Circuit Diagram]

a. Write a VHDL entity for the circuit.
b. Write a Boolean algebra expression for $Z$ and a VHDL dataflow architecture.
c. Write separate VHDL entities and dataflow architectures for the NOR2 and NOR3 components.
d. Write a VHDL structural architecture for the circuit using the components from Part c.